What is claimed is:

1. A dual port semiconductor memory device comprising:

a semiconductor substrate which includes a plurality of memory cells each memory cell is divided into first and second n-wells where P+ active regions are formed and first and second p-wells where N+ active regions are formed;

a wordline and a scan address line; and

a pair of bitlines comprised of a bitline and a complementary bitline and a scan data-out line,

wherein each of the plurality of memory cells comprising:

a first CMOS inverter which includes a first NMOS transistor, a first PMOS transistor, an input port, and an output port;

a second CMOS inverter which includes a second NMOS transistor, a second PMOS transistor, an input port, which is connected to the output port of the first CMOS inverter and constitutes a first memory node together with the output port of the first CMOS inverter, and an output port, which is connected to the input port of the first CMOS inverter and constitutes a second memory node together with the input port of the first CMOS inverter;

a third NMOS transistor a gate of which is connected to the wordline, a drain of which is connected to the bitline, and a source of which is connected to the first memory node;

a fourth NMOS transistor a gate of which is connected to the wordline, a drain of which is connected to the complementary bitline, and a source of which is connected to the second memory node; and

a third PMOS transistor a gate of which is connected to the scan address line, a source of which is connected to the second memory node, and a drain of which is connected to the scan data-out line,

wherein the first and third NMOS transistors are formed in the N+ active regions of the first p-well, the second and fourth NMOS transistors are formed in the N+ active regions of the second p-well, the first and second PMOS transistors are formed in the

P+ regions of the first n-well, and the third PMOS transistor is formed in the P+ active region of the second n-well.

2. The dual port semiconductor memory device of claim 1, wherein the plurality of memory cells are arranged in symmetry with respect to boundaries thereamong.

3. The dual port semiconductor memory device of claim 1, wherein the first p-well, the second p-well, the first n-well, and the second n-well are arranged on the semiconductor substrate in an alternating manner.

4. The dual port semiconductor memory device of claim 3, wherein the pair of bitlines and the scan data-out line are arranged in parallel with boundaries among the first and second p-wells and the first and second n-wells.

5. The dual port semiconductor memory device of claim 3, wherein the wordline and the scan address line are arranged in perpendicular to the boundaries among the first and second p-wells and the first and second n-wells.

6. The dual port semiconductor memory device of claim 1, further comprising wiring layers, which have fixed voltage potentials and are arranged on the same layer as the pair of bitlines are.

7. The dual port semiconductor memory device of claim 6, wherein the bitline, the complementary bitline, and the wiring layers are arranged in an alternating manner.

8. The dual port semiconductor memory device of claim 7, wherein a wiring layer that is arranged between the bitline and the complementary bitline is a power supply line.

9. A dual port semiconductor memory device comprising:

a semiconductor substrate which is divided into first and second n-wells in which P+ active regions are formed and first and second p-wells where N+ active regions are formed, the second p-well being located between the first and second n-wells and the first and second p-wells including a plurality of memory cells located at either side of the first n-well;

a wordline and a scan address line; and

a pair of bitlines, comprised of a bitline and a complementary bitline, and a scan data-out line,

wherein each of the plurality of memory cells comprising:

a first CMOS inverter which includes a first NMOS transistor, a first PMOS transistor, an input port, and an output port;

a second CMOS inverter which includes a second NMOS transistor , a second PMOS transistor, an input port, which is connected to the output port of the first CMOS inverter and constitutes a first memory node together with the output port of the first CMOS inverter, and an output port, which is connected to the input port of the first CMOS inverter and constitutes a second memory node together with the input port of the first CMOS inverter;

a third NMOS transistor a gate of which is connected to the wordline, a drain of which is connected to the bitline, and a source of which is connected to the first memory node;

a fourth NMOS transistor a gate of which is connected to the wordline, a drain of which is connected to the complementary bitline, and a source of which is connected to the second memory node; and

a third PMOS transistor a gate of which is connected to the scan address line, a source of which is connected to the second memory node, and a drain of which is connected to the scan data-out line,

wherein the first and third NMOS transistors are formed in the N+ active regions of the first p-well, the second and fourth NMOS transistors are formed in the N+ active regions of the second p-well, the first and second PMOS transistors are formed in the P+ regions of the first n-well, and the third PMOS transistor is formed in the P+ active region of the second n-well.

10. The dual port semiconductor memory device of claim 9, wherein the plurality of memory cells are arranged in symmetry with respect to boundaries thereamong.

11. The dual port semiconductor memory device of claim 9, wherein the pair of bitlines and the scan data-out line are arranged in parallel with boundaries among the first and second p-wells and the first and second n-wells.

12. The dual port semiconductor memory device of claim 9, wherein the wordline and the scan address line are arranged in perpendicular to the boundaries among the first and second p-wells and the first and second n-wells.

13. The dual port semiconductor memory device of claim 9, further comprising wiring layers, which have fixed voltage potentials and are arranged on the same layer as the pair of bitlines are.

14. The dual port semiconductor memory device of claim 13, wherein the bitline, the complementary bitline, and the wiring layers are arranged in an alternating manner.

15. The dual port semiconductor memory device of claim 14, wherein a wiring layer that is arranged between the bitline and the complementary bitline is a power supply line.

16. A dual port semiconductor memory device comprising:

a memory cell array unit in which a plurality of memory cells included in the dual port semiconductor memory device of claim 1 are arranged in a matrix form;

a plurality of wordlines and a plurality of scan address lines;

a plurality of pairs of bitlines, comprised of bitlines and complementary bitlines, and a plurality of scan data-out lines;

a read/write row decoder unit which selects one from among the plurality of wordlines;

a scan row decoder unit which selects one from among the plurality of scan address lines;

a column decoder unit which selects one from among the plurality of pairs of bitlines;

a scan latch circuit unit which latches data output to the plurality of scan data-out lines and thus generates scan output signals;

a precharge circuit unit which precharges the plurality of pairs of bitlines;

a predischarge circuit unit which predischarges the plurality of scan data-out lines;

a data input/output gate unit which inputs and outputs data to the plurality of pairs of bitlines;

a sense amplifier unit which amplifies a voltage difference between each of the plurality of bitlines; and

a data input/output circuit unit which generates output data using data output from the sense amplifier unit and outputs input data to the data input/output gate unit.

17. The dual port semiconductor memory device of claim 16, further comprising wiring layers, which have fixed voltage potentials and are arranged on the same layer as the pair of bitlines are.

18. The dual port semiconductor memory device of claim 17, wherein the bitline, the complementary bitline, and the wiring layers are arranged in an alternating manner.

19. The dual port semiconductor memory device of claim 18, wherein a wiring layer that is arranged between the bitline and the complementary bitline is a power supply line.

20. The dual port semiconductor memory device of claim 16 being mounted on a liquid crystal display integrated circuit (LDI).

21. A dual port semiconductor memory device comprising:

a memory cell array unit in which a plurality of memory cells included in the dual port semiconductor memory device of claim 9 are arranged in a matrix form;

a plurality of wordlines and a plurality of scan address lines;

a plurality of pairs of bitlines, comprised of bitlines and complementary bitlines, and a plurality of scan data-out lines;

a read/write row decoder unit which selects one from among the plurality of wordlines;

a scan row decoder unit which selects one from among the plurality of scan address lines;

a column decoder unit which selects one from among the plurality of pairs of bitlines;

a scan latch circuit unit which latches data output to the plurality of scan data-out lines and thus generates scan output signals;

a precharge circuit unit which precharges the plurality of pairs of bitlines;

a predischarge circuit unit which predischarges the plurality of scan data-out lines;

a data input/output gate unit which inputs and outputs data to the plurality of pairs of bitlines;

a sense amplifier unit which amplifies a voltage difference between each of the plurality of bitlines; and

a data input/output circuit unit which generates output data using data output from the sense amplifier unit and outputs input data to the data input/output gate unit.

22. The dual port semiconductor memory device of claim 21, further comprising wiring layers, which have fixed voltage potentials and are arranged on the same layer as the pair of bitlines are.

23. The dual port semiconductor memory device of claim 21, wherein the bitline, the complementary bitline, and the wiring layers are arranged in an alternating manner.

24. The dual port semiconductor memory device of claim 23, wherein a wiring layer that is arranged between the bitline and the complementary bitline is a power supply line.

25. The dual port semiconductor memory device of claim 21 being mounted on an LDI.